REMARKS

Applicant respectfully requests favorable reconsideration of this application, as amended.

As a preliminary matter, Applicant respectfully requests that the Examiner confirm receipt of the certified copy of the priority document, which was filed on October 17, 2001. A copy of the postcard receipt is attached. It is noted that the outstanding Office Action indicates that the priority document has not been received by the Office.

The specification and the drawings have been amended to correct minor errors. Regarding the drawings, see the accompanying Letter Proposing Drawing Changes.

Turning to the merits, Claim 1 has been amended and new Claims 17-20 have been presented in order to address certain preferred aspects of Applicant's invention with greater particularity. Claims 2-16 have been cancelled without prejudice or disclaimer. For the Examiner's convenience, it is noted that amended Claim 1 is exemplified by the first embodiment of the invention shown in Fig. 1. Claim 17 is exemplified by the third embodiment shown in Fig. 4. Claims 18 and 19 are exemplified by the fifth embodiment shown in Fig. 6, and Claim 20 is exemplified by the eighth embodiment shown in Fig. 11.

Applicant respectfully submits that each of the claims now presented distinguishes patentably from Giles et al., which was cited as the basis for the outstanding rejection under 35 U.S.C. § 102(b). The Giles circuit uses a pair of gate/latch arrangements 52,19 and 54,21 for the scan output signal and logic output signal, respectively. These arrangements are both controlled by the control (scan-enable) signal SE.

In contrast to Giles, in Applicant's storage circuit as set forth in Claim 1, for example, the output signal (third signal) from the first storage element is itself output through a first output of the storage circuit without being controlled by the control signal (see the scan-out signal line in Fig. 1). It is therefore unnecessary to provide a gate between the first storage element and the first output, and this allows for a reduction of the area of a chip on which the storage circuit is formed. Giles neither teaches nor suggests the arrangement of Claim 1.

Claim 17 distinguishes from Giles in that, inter alia, the slave latch passes the output signal of the master latch to the first output of the storage circuit in response to an inverted clock signal without being

controlled by the control signal (see slave latch g502 in Fig. 4). As previously noted, both of Giles's output gate arrangements are controlled by the control signal (scan enable signal).

Claim 18 is similar to amended Claim 1 in that the output signal (third signal) from the first storage element is output through a first output of the storage circuit without being controlled by the control signal. Thus, Claim 18 also distinguishes from Giles on this basis. But Claim 18 further distinguishes from Giles in that the fixing of the second logic output gate signal is in response to a second control signal. See Claim 18, lines 11-14.

Claim 20 distinguishes from Giles at least for reasons similar to those discussed above with respect to Claim 1. For example, note the features recited in the paragraph at lines 28-32.

This application is believed to be in condition for allowance for the reasons indicated above.

Accordingly, an early Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§

1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

MWS:jab

Miles & Stockbridge P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

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Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient potage as first class mail in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231 on November 25, 2002.

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Mitchell W. Shapiro

MARKED-UP COPY OF THE CLAIM:

1. (Amended) A storage circuit comprising:

a first logic gate for receiving a first signal and a second signal, and for selectively outputting either the first signal or the second signal in accordance with a control signal;

a first storage element for receiving a clock signal, for storing an output signal of the first logic gate in response to the clock signal, and for outputting the stored signal as a third signal in response to the clock signal; and

a second logic gate for receiving [an output] the third signal [of] from the first storage element, [and for outputting or] said second logic gate fixing [the] an output signal thereof, regardless of the received third signal, [of the first storage element] in response to the control signal;

wherein the storage circuit, having a first output and a second output, outputs the third signal through the first output, and the output signal of the second logic gate through the second output.

that it is possible to reduce the time required for the scan-mode operation.

The clock signal and the scan-enable signal may be supplied from the outside of the chip by using a tester, or may be produced within the chip by using an oscillation circuit added with a counter. Accordingly, by using the present configuration, it is possible to improve the frequency of the scan-mode operation without causing the fault detection mistake due to the excessive voltage drop or the chip destruction due to the heat generation, so that the test time can be reduced. In the first embodiment, since it is only required to add one logic gate for fixing the output signal to logic circuit g104 to each of the scan FFs, the increase of the chip area can be suppressed to a small amount. According to the inventors' study, it has been found that the increase of the chip area can be reduced to about 1%.

Fig. 3 is a circuit configuration diagram showing a semiconductor integrated circuit according to the second embodiment of the present invention. This is an example in which the function of the logic gate for fixing the output signal to logic circuit g104 described in the first embodiment is incorporated into the inside of the MUX-type scan FF. In this configuration, the output terminal is divided into a scan-out terminal and a logic output terminal. Further, before the logic output terminal, a 2-input

NOR gate g303 which is controlled by a scan-enable signal line n301 and a signal line n302 with inverse polarity to the logic output is inserted. By forming in such a configuration, as compared with the first embodiment, the number of the gate stages present on the path from a system clock terminal to a logic output terminal can be reduced. In other words, the number of the gate stages on the path from the signal line [n302] to the logic output terminal is two stages (the NOR gate g304 (in the conventional MUX-type scan FF, the scan-out terminal shown in Fig. 3 is the only output terminal) and the AND gate g104) [in the first embodiment], but there is only one stage (the NOR gate g303) in the present embodiment. Accordingly, by applying the present invention, the delay of the user logic circuit can be made smaller. Furthermore, since it is possible to reduce the size of the transistor forming the scan FF as compared with the first embodiment, the chip area reduction effect and the power consumption reduction effect can be expected.

It should be noted that the configuration of the present invention is not limited to the configuration mentioned above. For example, in Fig. 1, it is possible to use a transfer gate in place of the 2-input AND gate g104. In this case, there is an advantage that the chip area can be made smaller.

Fig. 4 is a circuit configuration diagram showing a semiconductor integrated circuit according to

inserted.

Fig. 6 is a circuit configuration diagram showing a semiconductor integrated circuit according to the fifth embodiment of the present invention. This is an example, in which in order to control the logic gate for fixing the output signal to logic circuit g104 described in the first embodiment, a logic output release line n701 is provided instead of the scan-enable signal line n103.

Fig. 7 is a timing chart showing the operation of the fifth embodiment. At the time of the transition from the scan-in operation to the logic test operation, it is possible to perform the release to fix the output signal to logic circuit, which is needed in the first embodiment, in parallel with the scan-in operation by setting the signal for fixing the output signal to logic circuit to "LOW" (s801) earlier than the scan-enable signal [s802]. For this reason, it becomes unnecessary to stop the clock signal transition (s802). Accordingly, there is an advantage that the test time can be reduced as compared with the first embodiment. Also, in the case of performing the burn-in test, the user logic circuit is operated with higher operating probability than that at normal operation. According to the present configuration, at burn-in, it becomes possible to operate the user logic circuit while inputting the signal to the scan FF.

Fig. 8 is a circuit configuration diagram

fix the output-to-logic signal described in Fig. 13, the assignment of scan FF able to fix the scan-out signal described in Fig. 14, and the external interface control are stored in a memory. Also, data expressing the RTL-level design description, the cell library, the gate-level netlist, the information of functional relationship between scan FF and normal FF described in Figs. 13 and 14, and the netlist with physical layout information are stored in the disc. Each of the programs can be manipulated and implemented by input from a keyboard or a mouse. Also, it is possible to refer to the implementation results of the respective programs by outputting them to a display. Also, all the stored programs and data can be preserved by a storage medium such as a compact disc.

Fig. 17 is a diagram showing a flow for designing a semiconductor integrated circuit to which the present invention is applied. In this flow, an LSI design foundry implements the design in which the normal scan FF and the scan FF of the present invention are mixed (hereinafter, referred to as "mixed design by using this scan flipflop"). In the present embodiment, a client of LSI design provides the LSI design foundry with only the design specifications. In this diagram, the black thick line indicates a dependence relationship between the processing and the information, and the arrow of white blank indicates the flow of the information. Specifically, the LSI design

foundary implements the mixed design by using this scan flipflop d2402 by using a design specifications d2401 provided by the client of LSI design, the cell library d1803 provided by a semiconductor foundary (performs the manufacture of the designed semiconductor integrated circuit), and the information of functional relationship between scan flipflop and normal flipflop d1804. Ultimately, the LSI design foundary prepares a gate-level netlist (hereinafter, referred to as "netlist using this scan flipflop") d2403. The prepared gate-level netlist d2403 is passed to the client of LSI design. In this respect, there will be a case where the cell library d1803 is also passed to the client of LSI design.

Fig. 18 shows an example in which the LSI design foundary implements the mixed design by using this scan flipflop. In this embodiment, there is shown a handling in which the client of LSI design (also performs the manufacture of the designed semiconductor integrated circuit) provides the LSI design foundary with not only the design specifications but also the cell library, and the gate-level netlist. In this diagram, the black thick line indicates the dependence relationship between the processing and the information, and the arrow of white blank indicates the flow of the information. Specifically, the LSI design foundary implements the mixed design by using this scan flipflop d2402 by using the design specifications

d2401, the cell library d1803, the information of functional relationship between scan flipflop and normal flipflop d1804 and the gate-level netlist not using the scan FF of the present invention (hereinafter, referred to as "netlist without this scan FF") d2501 all of which are provided by the client of LSI design. Ultimately, the LSI design foundary prepares the netlist using this scan FF d2403. Thereafter, the netlist d2403 is passed to the client of LSI design.

The semiconductor foundary (Fig. 17) or the client of LSI design (Fig. 18) reflects the mask pattern of physical layout prepared from the netlist to a semiconductor wafer (j2404). The logic test is performed on a semiconductor integrated circuit apparatus prepared after being reflected with the mask pattern of physical layout (j2405). Here, at logic test, the same frequency can be used for the scan-in operation, the logic test operation and the scan-out operation. In particular, it is desirable to use the same frequency as the clock frequency at normal operation. With respect to the user logic circuit portion using the normal scan FF, there is a problem of the heat generation and the like due to the rise of the operating probability. However, since it is possible to make such a portion occupy a very small portion in the semiconductor integrated circuit, no drawback is caused due to the semiconductor integrated circuit

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Applicant: Ichiro KONO T3351-907474
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Attached: Transmittal of Certified Copy of Priority Document;
Certified Copy of JP 2000-350553.

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